Payman Zarkesh-Ha
Associate Professor

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Employment

Associate Professor, Department of ECE, University of New Mexico, NM	2012–present
Assistant Professor, Department of ECE, University of New Mexico, NM	2006–2012
Senior Research Engineer, DSM Solutions Inc., Los Gatos, Calif.	2006–2009
Senior Research Engineer, LSI Logic Corporation, Milpitas, Calif.	2001–2006
Research Assistant, Georgia Institute of Technology, Atlanta, Georgia	1996–2001

Education

Georgia Institute of Technology, Atlanta, Georgia (Sept. 1996–March 2001)
Ph.D. in Electrical Engineering, Overall GPA of 4.0
Dissertation: *Global Interconnect Modeling for a Gigascale System-on-a-Chip (GSoC)*

Sharif University of Technology, Tehran, Iran (June 1992–June 1994)
M.S. in Electrical Engineering, Overall GPA of 3.8
Thesis: *An Analog High Frequency CMOS Monolithic Filter Using Sampled-Data Technique*

Iran University of Science and Technology, Tehran, Iran (Sept. 1988–June 1992)
B.S. in Electrical Engineering *(with honors)*, Overall GPA of 3.6

Research Interests

- **Analog and digital VLSI circuit designs**
- **High-performance and low-power VLSI designs**
- **Statistical modeling of VLSI systems**
- **Fault tolerance and yield enhancement design techniques**
- **Novel nanoelectronic devices such CNFETs**

Professional Activities and Services

- Author or co-author of over 60 peer-reviewed journals and conference proceedings including *IEEE transactions on VLSI systems, IEEE Transactions on Electron Devices, The IBM Journal of Research and Development, Symposium on VLSI Technology, IEEE International Solid-State Circuits Conference (ISSCC),* and *Custom Integrated Circuit Conference (CICC)*
- Inventor or co-inventor of procedures resulting in 12 patents (ten issued, two pending)
- Author of a book chapter and coauthor of a book.
- Served as industry liaison for LSI Logic corporation with *Semiconductor Research Corporation* (SRC) and *Microelectronics Advanced Research Corporation* (MARCO) from 2001 to 2006
- Serving as reviewer of several articles submitted for publication in top-ranked journals and conferences such as *Science Magazine*, *IEEE transactions on VLSI systems*, and *Design Automation Conference (DAC)*
- Serving as technical program committee member of *System Level Interconnect Prediction (SLIP)* since 2001
- Serving as technical program committee member of the *IEEE International Symposium on Quality Electronic Design (ISQED)* since 2009

Professional Membership

- **Senior Member**, Institute of Electrical and Electronics Engineers (IEEE)
- **Member**, Association for Computing Machinery (ACM)

Awards

- 1997, Prestigious Kharazmi National Science award for “Industrial Automation System”
- 1997, Gamma Beta Phi Honor Society
- 2003/2005, LSI Logic’s Best Author/Inventor Award
- 2009, ECE Outstanding Teacher Award

University Services

- **Member, ECE Faculty Search Committee (CompE), 2010**
- **Chair, ECE Security Committee, Feb. 2008 – Present**
- **Member, ECE Computer Usage Committee (CUC), Oct. 2006 – Present**
- **Member, ECE Faculty Search Committee (CompE), 2008**
- **Chair, Microelectronics Area, 2008 – Present**
- **Member, ECE CompE Faculty Committee, 2006 - Present**
- **Member, ECE Graduate Committee, 2006-2007**
- **Member, ECE Undergraduate Committee, 2007-2012**
- **Member, ECE EYES Program Committee, 2006-2007**

Teaching

- **ECE 638**, Special Topic: VLSI Testing
- **ECE 595**, Advanced VLSI Design
- **ECE 520/424**, VLSI Design
- **ECE 523/421**, Analog Electronics
- **ECE 321**, Electronics I
- **ECE 203**, Circuit Analysis I

Current Students

- **Ph.D. students:** James Harmon, Ali Arabi Shahi, Rakesh Mahto, and Javad Ghasemi
- **M.S. students (with Thesis):** Joshua Kotobi

Graduated Students

- **M.S. students (with Thesis):** Rani A. Ghaida, Aahlad Mallajosyula, Jason Hamlet, Cameron Stark, Vallabh Srikanth Devarapalli, Naveen Nischal Purushotham, Anahita Khoshakhlagh, Manoj Kumar Ramalingam Rajasekaran, Jiawei Xu, and Thomas LeBoeuf

Grants and Contracts

- **National Science Foundation (NSF):** “A Reconfigurable Readout Circuit for Integrated Infrared Spectral Sensing,” PI: P. Zarkesh-Ha, Co-PIs: M. M. Hayat and S. Krishna; $450,000; Aug. 2009 – Aug. 2012.
- **Department of Energy (DoE):** “End-System Network Interface Controller for 100 Gb/s Wide Area Networks,” PI: P. Zarkesh-Ha, $450,000, Collaborator: Acadia Optronics, Sept. 2009 – Sept. 2012.
- **Air Force Research Laboratory (AFRL):** “VLSI Chip Fabrication,” PI: P. Zarkesh-Ha, $87,500; June 2011 – June 2012.
- **Air Force Research Laboratory (AFRL-RVSE):** “Real-time Reconfigurable Systems for Space Applications,” PI: C. Christodoulou, Co-PIs: M. Pattichis, S. Jayaweera, and P. Zarkesh-Ha, $1,500,000; October 2008 – September 2013.
- **National Science Foundation (NSF- Smart Lighting Engineering Research Center):** “A novel LED/detector integrated circuit for smart lighting application,” Lead PI: B. Karlicek (RPI), Participant: P. Zarkesh-Ha; $65,125 in sub-award; Aug. 2010 – Aug. 2011 (Grant has been extended for 5 more years).
- **Air Force Office of Scientific Research (AFOSR):** “Adaptive Integrated Multi-Modal Sensing Array,” PI: S. Krishna, Participant: P. Zarkesh-Ha; $9,975 in sub-award; April 2011 – April 2012.

Book Publications

- Payman Zarkesh-Ha, "Power, Clock, and Global Signal Distribution," *chapter 5 in Interconnect Technology Design for Gigascale Integration*, Kluwer Academic Publishers, 2003.
- Charles Hawkins, Jaume Segura, and Payman Zarkesh-Ha, "*Introduction to Modern CMOS Digital Electronics*," SciTech Publishing, 2011.

Issued Patents

1. P. Wright, P. Zarkesh-Ha, "Flip Chip Testing," Patent No: US 6,617,181, Issued September 9, 2003.
2. P. Wright, P. Zarkesh-Ha, "Integrated circuit containing redundant core and peripheral contacts," Patent No: US 6,710,453, Issued March 23, 2004.
3. P. Zarkesh-Ha, K. Doniger, "Low-loss On-chip Transmission Line for Integrated Circuit Structures," Patent No: US 6,855,624, Issued February 15, 2005.
4. Q. Cui, B. Davis, S. Bhutani, P. Zarkesh-Ha, J. Corbil, P. Krishnamurthy, "Method of delay calculation for variation in interconnect metal process," Patent No: US 6,880,142, Issued April 12, 2005.
5. P. Zarkesh-Ha, W. Loh, C.H. Chang, "Field Programmable Platform Array (FPPA)," Patent No: 20050166170, Issued July 2005.
6. P. Zarkesh-Ha, W. Loh, "Energy Recycling in Clock Distribution Networks Using On-chip Inductors," Patent No: US 7,082,580, Issued July 25, 2006.
7. P. Zarkesh-Ha, K. Doniger, W. Loh, "A New Interconnect Routing Using Parallel Lines," Patent No: US 7,014,957, Issued March 21, 2006.
8. W. Loh, K. Doniger, P. Zarkesh-Ha, J. Chen, and C. Ito, "Circuit Protection System," Patent No: US 7,777,996, Issued August 17, 2010.
9. P. Zarkesh-Ha, S. Bhutani, W. Guo, "Probabilistic Noise Analysis," Patent No: US 7,661,083, Issued February 9, 2010.
10. P. Zarkesh-Ha, C. Hamlin; A. Kapoor; J. Koford; M. Vora; "System and Method for Routing Connections," Patent No: US 7,689,964, Issued March 30, 2010.

Publications

Total Citations=691, g-index=24, and h-index=15 (Based on Google Scholar, September 2011)

Journal Publications:

1. P. Zarkesh-Ha, J.A. Davis, and J.D. Meindl, "Prediction of Net-Length Distribution for Global Interconnects in a Heterogeneous System-on-a-Chip," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, pp. 649–659, Dec. 2000.
2. Q. Chen, J.A. Davis, P. Zarkesh-Ha, and J.D. Meindl, "A Compact Physical via Blockage Model," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, pp. 689–692, Dec. 2000.
3. J. Joyner, R. Venkastesan, P. Zarkesh-Ha, J.A. Davis, and J.D. Meindl, "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, pp. 922–928, Dec. 2001.
4. J. D. Meindl, J. Davis, P. Zarkesh-Ha, C.S. Patel, K Martin, and P.A. Kohl, "Interconnect Opportunities for Gigascale Integration," *IBM Journal of Research and Development*, vol. 46, pp. 245–263, May 2002.
5. J. Joyner, P. Zarkesh-Ha, and J.D. Meindl, "Global Interconnect Design in a Three-Dimensional System-on-a-Chip," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, pp. 367–372, April 2004.
6. P. Zarkesh-Ha and K. Doniger, "Interconnect Layout Sensitivity and Yield Prediction," *Electronic Device Failure Analysis Magazine*, pp. 6-13, Feb. 2007.
7. R. Ghaida and P. Zarkesh-Ha, "A Layout Sensitivity Model for Estimating Electromigration-vulnerable Narrow Interconnects," *Journal of Electronic Testing, Springer*, July 2008.
8. R. Ghaida, K Doniger, and P. Zarkesh-Ha, "Random Yield Prediction Based on a Stochastic Layout Sensitivity Model," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, issue 3, pp. 329-337, August 2009.

9. P. Zarkesh-Ha and A. Shahi, “Stochastic Analysis and Design Guidelines for CNFETs in Gigascale Integrated Systems,” *IEEE Transactions on Electron Devices*, vol. 58, issue 2, pp. 530-539, Feb. 2011.
10. W. Y. Jang, M. Hayat, S. Godoy, S. Bender, P. Zarkesh-Ha, and S. Krishna, “Data Compressive Paradigm for Multispectral Sensing using Tunable DWELL Mid-infrared Detectors,” *Optics Express*, vol. 19, issue 20, pp. 19454–19472, September 2011.
11. W-Y Jang, M. M. Hayat, P. Zarkesh-Ha, and S. Krishna, "Continuous time-varying biasing approach for spectrally tunable infrared detectors," Optics Express, vol. 20, no. 28, pp. 29823-29836, 2012

Conference Publications:

1. P. Zarkesh-Ha and J.D. Meindl, “Stochastic Net-Length Distributions for Global Interconnects in a Heterogeneous System-on-a-Chip,” *IEEE Symposium on VLSI Technology*, pp. 44–45, June 1998.
2. P. Zarkesh-Ha, J.A. Davis, W. Loh, and J.D. Meindl, “On a Pin versus Gate Relationship for Heterogeneous Systems: Heterogeneous Rent’s Rule,” *IEEE Custom Integrated Circuit Conference*, pp. 93–96, May 1998.
3. P. Zarkesh-Ha, J.A. Davis, W. Loh, and J.D. Meindl, “Stochastic Interconnect Network Fan-out Distribution Using Rent’s Rule,” *IEEE International Interconnect Technology Conference*, pp. 184–186, June 1998.
4. P. Zarkesh-Ha, T. Mule, and J.D. Meindl, “Characterization and Modeling of Clock Skew with Process Variations,” *IEEE Custom Integrated Circuit Conference*, pp. 441–444, May 1999.
5. P. Zarkesh-Ha and J.D. Meindl, “Optimum Chip Clock Distribution Networks,” *IEEE International Interconnect Technology Conference*, pp. 18–20, May 1999.
6. P. Zarkesh-Ha, P. Bendix, W. Loh, J. Lee, and J.D. Meindl, “The Impact of Cu/Low k on Chip Performance,” *IEEE International ASIC/SoC Conference*, pp. 257–261, Sep. 1999.
7. P. Zarkesh-Ha and J.D. Meindl, “Asymptotically Zero Power Dissipation Gigahertz Clock Distribution Networks,” *IEEE Electrical Performance and Electronic Packaging*, pp. 57–60, Oct. 1999.
8. P. Zarkesh-Ha and J.D. Meindl, “An Integrated Architecture for Global Interconnects in a Gigascale System-on-a-Chip (GSoC),” *IEEE Symposium on VLSI Technology*, pp. 194–195, June 2000.
9. P. Zarkesh-Ha, J.A. Davis, W. Loh, and J.D. Meindl, “Prediction of Interconnect Fan-out Distribution Using Rent’s Rule,” *International Workshop on the System-Level Interconnect Prediction*, pp. 107–112, April 2000.
10. J. Joyner, P. Zarkesh-Ha, J.A. Davis, and J.D. Meindl, “A Three-Dimensional Stochastic Wire-Length Distribution for Variable Separation of Strata,” *IEEE International Interconnect Technology Conference*, pp. 126–128, June 2000.
11. A. Naeemi, P. Zarkesh-Ha, C. Patel, and J.D. Meindl, “Performance Improvement using On-Board Wires for On-Chip Interconnects,” *IEEE Electrical Performance and Electronic Packaging*, pp. 325–328, Oct. 2000.
12. P. Zarkesh-Ha and J.D. Meindl, “An Integrated Architecture for Global Interconnects in a Gigascale System-on-a-Chip (GSoC),” Proceedings of the 12th *International Conference on Microelectronics*, pp. 149–152, Nov. 2000.
13. Q. Chen, J.A. Davis, P. Zarkesh-Ha, and J.D. Meindl, “A Novel Via Blockage Model and Its Implications,” *IEEE International Interconnect Technology Conference*, pp. 15–17, June 2000.
14. J. Joyner, P. Zarkesh-Ha, J.A. Davis, and J.D. Meindl, “Vertical Pitch Limitations on Performance Enhancement in Bonded Three-Dimensional Interconnect Architectures,” *International Workshop on the System-Level Interconnect Prediction*, pp. 123–127, April 2000.
15. P. Zarkesh-Ha and J.D. Meindl, “An Integrated Architecture for Global Interconnects in a Gigascale System-on-a-Chip (GSoC),” *TECHCON’00*, Sept. 2000.
16. P. Zarkesh-Ha and J.D. Meindl, “Optimum On-Chip Power Distribution Networks for Gigascale Integration (GSI),” *IEEE International Interconnect Technology Conference*, pp. 125–127, June 2001.
17. J. Joyner, P. Zarkesh-Ha, and J.D. Meindl, “A Global Interconnect Design Window for a Three-Dimensional System-on-a-Chip,” *IEEE International Interconnect Technology Conference*, pp. 154–156, June 2001.
18. A. Naeemi, C. Patel, M. Bakir, P. Zarkesh-Ha, K. Martin, and J.D. Meindl, “Sea of Leads: a Disruptive Paradigm for System-on-a-Chip (SoC),” *IEEE Solid State Circuit Conference*, pp. 280–281, Feb. 2001.

19. M. Saint-Laurent, P. Zarkesh-Ha, M. Swaminathan, and J.D. Meindl, "Optimal Clock Distribution with an Array of Phase-Locked Loops for Multiprocessor Chips," Proceedings of the 44th *IEEE Midwest Symposium on Circuits and Systems*, pp. 127–131, August 2001.

20. P. Zarkesh-Ha, W. Loh, P. Bendix, and J.D. Meindl, "Optimum Interconnect Design for ASIC Chips," *VLSI Multilevel Interconnection Conference (VMIC)*, pp. 407–412, Nov. 2001.

21. J. Joyner, P. Zarkesh-Ha, and J.D. Meindl, "A Stochastic Global Net-Length Distribution for a Three-Dimensional system-on-a-Chip (3D-SoC)," *IEEE International ASIC/SoC Conference*, pp. 147–151, Sept. 2001.

22. J. D. Meindl, R. Venkatesan, J. Davis, J. Joyner, A. Naeemi, P. Zarkesh-Ha, M. Bakir, T. Mule, P. Kohl, and K. Martin, "Interconnecting Device Opportunities for Gigascale Integration (GSI)," *IEEE International Electron Device Meeting*, pp. 525–528, Dec. 2001.

23. P. Zarkesh-Ha, P. Wright, S. Lakshminarayanan, C-C Cheng, W. Loh, and W. Lynch, "Backend Process Optimization for 90nm High-Density ASIC Chips," *IEEE International Interconnect Technology Conference (IITC)*, pp. 123–125, June 2003.

24. V. Sukharev, P. Zarkesh-Ha, C.H. Chang, W. Loh, and K. Zhang, "Metal Density Optimization With CMP-Based Dummy Placement," *International CMP Planarization for ULSI Multilevel Interconnection Conference (CMP-MIC)*, pp. 453–462, February 2003. **(invited talk)**

25. P. Zarkesh-Ha, S. Lakshminarayann, K. Doniger, W. Loh, and P. Wright, "Impact of Interconnect Pattern Density Information on a 90nm Technology ASIC Design Flow," *International Symposium on Quality Electronic Design (ISQED)*, pp. 405–409, March 2003.

26. P. Zarkesh-Ha, K. Doniger, W. Loh, and P. Wright, "Prediction of Interconnect Pattern Density Distribution: Derivation, Validation, and Applications," *International Workshop on the System-Level Interconnect Prediction (SLIP)*, pp. 85–91, April 2003.

27. P. Zarkesh-Ha, P. Burke, K. Doniger, W. Loh, V. Sukharev, M. Lu, P. Bendix, W. Catabay, W.J. Hsia, and C.H. Chang, "Influence of Ultra Low k Dielectric on the Performance of Integrated Circuit Down to 45 nm Technology Node," *International VLSI/ULSI, Multilevel Interconnect Conference (VMIC)*, pp. 17–31, September 2003. **(invited talk)**

28. P. Zarkesh-Ha, K. Doniger, W. Loh, D. Sun, R. Stephani, and G. Priebe, "A Compact Model for Analysis and Design of On-chip Power Network with Decoupling Capacitors," *International Conference on Computer Design (ICCD)*, pp. 84–89, October 2003.

29. P. Zarkesh-Ha, K. Doniger, W. Loh, and P. Bendix, "Prediction of Interconnect Adjacency Distribution, Validation, and Applications," *International Workshop on the System Level Interconnect Prediction (SLIP)*, pp. 99-106, Feb. 2004.

30. P. Zarkesh-Ha and K. Doniger, "Stochastic Interconnect Layout Sensitivity Model," *IEEE International Workshop on the System-Level Interconnect Prediction*, pp. 9-14, March 2007.

31. R. Sarvari, A. Naeemi, P. Zarkesh-Ha, and J. Meindl, "Design and Optimization for Nanoscale Power Distribution Networks in Gigascale Systems," *IEEE International Interconnect Technology Conference (IITC)*, pp. 190-192, June 2007.

32. C. Hawkins, P. Zarkesh-Ha, J. Segura, "Little Vias can be Vicious," *13th NASA Symposium on VLSI Design*, June 2007.

33. R. Abou Ghaida and P. Zarkesh-Ha, "Estimation of Electromigration-Aggravating Narrow Interconnects Using a Layout Sensitivity Model," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, pp. 59-67, September 2007.

34. V. Jain and P. Zarkesh-Ha, "Analytical Noise-Rejection Model Based on Short Channel MOSFET", *International Symposium on Quality Electronic Design (ISQED)*, pp. 401-406, March 2008.

35. A. Mallajosyula and P. Zarkesh-Ha, "A Very Low Overhead Method to Filter Single Event Transients in Combinational Logic," *IEEE Workshop on Silicon Errors in Logic System Effects (SELSE)*, March 2008.

36. A. Mallajosyula and P. Zarkesh-Ha, "A Robust Single Event Upset Hardened Clock Distribution Network," *IEEE International Integrated Reliability Workshop (IIRW)*, October 2008.

37. S. Devarapalli, P. Zarkesh-Ha, and S. Suddarth, "Adaptive Circuit Implementation in FPGAs," *FPGA Summit*, Dec. 2008.

38. V.S. Devarapalli, P. Zarkesh-Ha, and S. Suddarth, "Scavenger: An Adaptive Design Technique for Low Power ASIC/FPGA," *IEEE International Conference on Computing, Engineering, and Information*, pp.164-167, April 2009.

39. P. Zarkesh-Ha and A. Shahi, "Logic Gate Failure Characterization for Nanoelectronic EDA Tools," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS)*, pp. 16-23, Oct. 2010.

40. S. Devarapalli, P. Zarkesh-Ha, and S. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using c-elements," *International Symposium on Quality Electronic Design (ISQED)*, pp. 147-150, March 2010.

41. S. Devarapalli, P. Zarkesh-Ha, and S. Suddarth, "SEU-Hardened Dual Data Rate Flip-Flop Using C-Elements," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS)*, pp. 167-171, Oct. 2010.

42. A. Atghiaee, N. Masoumi, and P. Zarkesh-Ha, "Nano-scale Early-Design-Stage Prediction for Crosstalk-Induced Power," *International Nanoelectronics Conference (INEC)*, pp. 585-586 , Jan. 2010.

43. P. Zarkesh-Ha, W. Jang, P. Nguyen, A. Khoshakhlagh, and J. Xu, "A Reconfigurable ROIC for Integrated Infrared Spectral Sensing," *23rd Annual Meeting of the IEEE Photonic Society*, pp. 714-715, Nov. 2010.

44. N. Purushotham, S. Devarapalli. J. Lyke, and P. Zarkesh-Ha, "Self-Healing Adjustable Memory System," *American Institute of Aeronautics and Astronautics*, AIAA 2010-3373, April 2010.

45. G. Bezerra, S. Forrest, M. Moses, A. Davis, and P. Zarkesh-Ha, "Modeling NoC Traffic Locality and Energy Consumption with Rent's Communication Probability Distribution," *IEEE System Level Interconnect Prediction (SLIP) Workshop*, pp. 3-8, June 2010.

46. P. Zarkesh-Ha, G. Bezerra, S. Forrest, and M. Moses, "Hybrid Network on Chip (HNoC): Local Buses with a Global Mesh Architecture," *IEEE System Level Interconnect Prediction (SLIP) Workshop*, pp. 9-14, June 2010.

47. R. Helinski, T. LeBoeuf, C. Hoffman, and P. Zarkesh-Ha, "A Linear Digital VCO for Clock Data Recovery (CDR) Applications," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 98-101, Dec. 2010.

48. P. Zarkesh-Ha, "A Novel LED/Detector Integrated Circuit," *World Scientific and Engineering Academy and Society (WSEAS) Conferences*, March 2011. **(invited talk)**

49. G. Bezerra, S. Forrest, and P. Zarkesh-Ha, "Reducing Energy and Increasing Performance with Traffic Optimization in Many-core Systems," *IEEE System Level Interconnect Prediction (SLIP) Workshop*, June 2011.

50. J. Xu, G. Fiorante, P. Zarkesh-Ha, and S. Krishna, "A Readout Integrated Circuit (ROIC) with Hybrid Source/Sensor Array," to appear at the *Annual Meeting of the IEEE Photonic Society*, Oct. 2011.

51. Ali Arabi Shahi, P. Zarkesh-Ha, "Prediction of gate delay variation for CNFET under CNT density variation," IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp.140-145, Oct. 2012.

52. Ali Arabi Shahi, P. Zarkesh-Ha, M. Elahi, "Comparison of variations in MOSFET versus CNFET in gigascale integrated systems," 13th International Symposium on Quality Electronic Design (ISQED) pp.378-383, March 2012.